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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,429	10/15/2001	Michael J. Mezeul	131105.1011	5001

32914 7590 08/31/2007

GARDERE WYNNE SEWELL LLP
INTELLECTUAL PROPERTY SECTION
3000 THANKSGIVING TOWER
1601 ELM ST
DALLAS, TX 75201-4761

EXAMINER	
RYMAN, DANIEL J	
ART UNIT	**PAPER NUMBER**
2616	

MAIL DATE	DELIVERY MODE
08/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

T11

Office Action Summary	Application No.	Applicant(s)	
	09/978,429	MEZEUL ET AL.	
	Examiner	Art Unit	
	Daniel J. Ryman	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,12,13,25,28-30 and 32-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12,13,25,28-30 and 32-40* is/are rejected.

7)☒ Claim(s) *2,3,6-9,13,28-30 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/10/2007 have been fully considered but they are not persuasive. On page 9 of the Response, Applicant asserts that "*Shiota* teaches pushing a shim header 312, or rewriting the top of the packet within the buffer memory 313 but fails to teach pushing an internal routing label onto a label stack." Applicant further asserts that "output channel information (*Shiota* Figs. 8 and 10; Figs. 12 and 13) is not an internal routing label (*Application* Fig. 2, SIC)." Thus, Applicant asserts that the Shiota's output channel information is not an internal routing label. Examiner, respectfully, disagrees.

2. "During patent examination, the pending claims must be 'given their broadest reasonable interpretation consistent with the specification.'" MPEP § 2111 (citations omitted). While Examine recognizes that Applicant is free to be his or her own lexicographer by defining specific terms in the claims, any such definition must be set out explicitly in the specification. MPEP § 2111.01(IV) (citations omitted). In the present case, Applicant has failed to explicitly define the term "internal routing label" in the specification, such that Examiner is required to give this term its broadest reasonable interpretation consistent with the specification. The term "internal routing label" only requires a label that is used by a device internally for routing. Examiner submits that Shiota's output channel information reads on this interpretation of the term "internal routing label." Simply, Shiota's shim header is a label (col. 1, lines 28-30, where a label is merely an identifier indicating routing information, and col. 8, lines 43-55, where the output channel information identifies routing information, such that the output channel information, as broadly defined, is a "label") that is used by a device internally (Fig. 1, ref. 4, and col. 15, lines 26-37,

where a controller writes an "updated internal held header" to a packet before transferring it to the internal switch, col. 13, lines 38-48, where the internal held header includes output channel information, and col. 8, lines 43-55, where the internal switch uses the output channel information to route the packet to the correct line card, see also col. 8, lines 39-41, where the switch is internal to a router, i.e. LSR) for routing (col. 8, lines 43-55, where the internal switch uses the output channel information to route the packet to the correct line card). As such, Examiner maintains that Shiota's "output channel information" reads on the claimed "internal routing label."

3. Applicant further asserts on pages 9-12 of the Response that the secondary references Landegem, Timbs, and Shimojo fail to "compensate for the deficiency in *Shiota*." However, as outlined above, Examiner submits that there is no deficiency in Shiota with respect to the claimed "internal routing label" that these secondary references would need to compensate.

4. In view of the foregoing, Examiner maintains that the claims are obvious in view of the cited prior art.

Claim Objections

5. Claim 2 is objected to because of the following informalities: in lines 1-2, "routing the packet" should be "routing the modified packet". Appropriate correction is required.

6. Claim 3 is objected to because of the following informalities: in lines 1-2, "routing the packet" should be "routing the modified packet". Appropriate correction is required.

7. Claim 6 is objected to because of the following informalities: in lines 1-2, "routing the packet" should be "routing the modified packet" and, in line 2, "a plurality" should be "the plurality". Appropriate correction is required.

8. Claim 7 is objected to because of the following informalities: in lines 1-2, "routing the packet" should be "routing the modified packet"; in line 2, "a plurality" should be "the plurality"; in line 3, "the packet" should be "the modified packet"; in line 4, "the packet" should be "the modified packet"; and, in line 4, "a plurality" should be "the plurality". Appropriate correction is required.

9. Claim 8 is objected to because of the following informalities: in lines 1-2, "routing the packet" should be "routing the modified packet" and, in line 2, "a plurality" should be "the plurality". Appropriate correction is required.

10. Claim 9 is objected to because of the following informalities: in lines 1-2, "routing each packet" should be "routing the modified packet" since claim 32, upon which claim 9 depends, does not disclose multiple packets to thereby necessitate an "each" limitation; in line 2, "a processor" should be "the processor"; and, in line 4, "each packet" should be "the packet". Appropriate correction is required.

11. Claim 13 is objected to because of the following informalities: in line 2, "label information table stack" should be "label stack" since "the label information table stack" lacks antecedent basis. Appropriate correction is required.

12. Claim 28 is objected to because of the following informalities: in lines 1-2, "routing the packet" should be "routing the modified packet". Appropriate correction is required.

13. Claim 29 is objected to because of the following informalities: in lines 1-2, "routing the packet" should be "routing the modified packet" and, in line 6, "label for transporting the packet" should be "label" since "the routing label for transporting the packet" lacks antecedent basis. Appropriate correction is required.

14. Claim 30 is objected to because of the following informalities: in line 1, "claim 1" should be "claim 32" since "routing the packet to a processor and sending the reply packet" lacks antecedent basis in claim 1, and, in lines 1-2, "routing the packet" should be "routing the modified packet". Appropriate correction is required.

15. Claim 37 is objected to because of the following informalities: in line 2, "routing the packet" should be "routing the modified packet". Appropriate correction is required.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1, 13, 25, 28, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiota (USPN 6,987,762), of record, in view of van Landegem (USPN 5,265,091), of record.

18. Regarding claim 1, Shiota discloses a method of routing IP packets between a plurality of circuit cards within a node of a network (where the MPLS packet is an IP packet "encapsulated by the data called a shim header," col. 1, lines 26-28, and where the packets are routed between a plurality of circuit cards within a node, Fig. 1 and col. 8, lines 39-59), comprising: receiving a packet at an interface, the packet being an IP packet and including a label stack, the label stack including an external routing label for use in forwarding between nodes along a label switched path (col. 8, lines 39-59, where an MPLS packet is received and its label stack is processed); pushing an internal routing label to the label stack of the packet, the internal routing label

specifying one of a plurality of circuit cards (where a controller writes an "updated internal held header" to a packet, col. 15, lines 26-33, where the internal held header includes output channel information, col. 13, lines 38-48, and where the switch uses the output channel information to route the packet to the correct line card, col. 8, lines 43-55); routing the packet to the one of the plurality of circuit cards specified in the internal routing label (where a controller writes an "updated internal held header" to a packet, col. 15, lines 26-33, where the internal held header includes output channel information, col. 13, lines 38-48, and where the switch uses the output channel information to route the packet to the correct line card, col. 8, lines 43-55).

Shiota does not expressly disclose that the routing label includes a packet type where the routing of the packet to the one of the plurality of circuit cards specified in the label occurs in response to the packet type being indicative of a first type. Van Landegem discloses, in a system that utilizes an internal routing tag, having a control cell that includes a Type field (col. 8, lines 25-34). Van Landegem also discloses that the control cell is switched differently than normal cells in that the control cell is sent to a processor on the node (col. 9, lines 12-17), rather than a circuit card. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use van Langegem's control cell in the context of Shiota's switching node to permit the node to receive and process control packets. To do this, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the routing label include a packet type to allow the system to distinguish between "normal" packets and control packets thereby enabling the system to route normal packets to one of the plurality of circuit cards specified in the label and to route the control packet to a controller in the switching node.

19. Regarding claim 13, Shiota in view of van Landegem discloses popping the routing label from the label information table stack after receiving the packet at the processor within the system (van Landegem: col. 9, lines 18-22, where the processor determines the output link of the cell and where cell are routed according to routing tags such that the processor "pops" the label from an information table stack).

20. Regarding claim 25, Shiota in view of van Landegem discloses popping the routing label from the label stack after receiving the packet at the processor within the node system (van Landegem: col. 9, lines 45-61, where the processor modifies the routing label such that is "pops" the label before it modifies it).

21. Regarding claim 28, Shiota in view of van Landegem discloses receiving the packet at a switch (Shiota: Fig. 1 and col. 8, lines 51-55, where the switch receives packets from the line cards); and switching the packet to a predetermined port of the switch coupled to the one of the plurality of circuit cards specified in the routing label (Shiota: Fig. 1 and col. 8, lines 51-55, where the switch switches the packets to a respective line car based on the output channel information, i.e. "routing label").

22. Regarding claim 32, Shiota in view of van Landegem discloses routing the packet to a processor within the system in response to the packet type being indicative of a control packet (van Landegem: col. 9, lines 12-17, where the system routes a control packet to a processor) and sending a reply packet to the one of the plurality of circuit cards specified in the internal routing label (van Landegem: col. 10, lines 6-12 where a confirm control cell is sent to the sender to acknowledge the setup of the connection and Shiota: col. 2, lines 1-16, where the apparatus uses label switched paths, such that the combination of Shiota and van Landegem

suggests using control packets in the apparatus to set up label switched paths through the apparatus).

23. Claims 2-9, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiota (USPN 6,987,762), of record, in view of van Landegem (USPN 5,265,091), of record, as applied to claims 1 and 23 above, and further in view of Timbs (USPN 5,809,025), of record.

24. Regarding claims 2, 3, 6, 7, and 29, Shiota in view of van Landegem discloses that routing the packet to the one of a plurality of circuit cards comprises: receiving the packet at a switch (Shiota: col. 8, lines 39-59, where an MPLS packet is received and its label stack is processed); and switching the packet to the one of the plurality of circuit cards coupled to a predetermined port of the switch (Shiota: col. 8, lines 43-55, where the switch uses the output channel information to route the packet to the correct line card).

Shiota in view of van Landegem does not expressly disclose that the port is specified by a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label. Timbs teaches, in a system for switching information between cards, routing a cell upon an inter-shelf route by using a shelf identifier (BTSI shelf number) and a slot identifier (slot identification number) (col. 10, lines 13-18). Timbs further discloses that, once a cell is received upon a particular destination shelf, the cell is routed according to a link identifier (span line number) and a channel identifier (channel number) (col. 10, lines 24-36). Timbs teaches that routing according to a shelf identifier, a slot identifier, a link identifier, and a channel identifier is beneficial because this permits "near-static routing of a data stream" "with minimal requirements of shared resources" (col. 2, line 66-col. 3, line 3). Simply, in such a system, within the switch, each intermediate module will be able to switch a cell based on

static information contained in the module (col. 3, lines 7-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to switch packets according to a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label in the system of Shiota since such routing permits "near-static routing of a data stream" where this eases the burden on the switch to update the switching tables.

25. Regarding claims 4, 5, 8, 9, and 30, Shiota in view of van Landegem discloses that routing the packet to a processor and sending the reply packet comprises: receiving the packet at a switch (Shiota: col. 8, lines 39-59, where an MPLS packet is received and its label stack is processed); switching the packet to a predetermined port of the switch coupled to the processor (Shiota: col. 8, lines 43-55, where the switch uses the output channel information to route the packet to the correct line card); and switching the reply packet to the one of the plurality of circuit cards coupled to a second predetermined port of the switch (van Landegem: col. 10, lines 6-14, where the confirm control cell is routed according to a routing label).

Shiota in view of van Landegem does not expressly disclose that the port is specified by a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label. Timbs teaches, in a system for switching cells between cards, routing a cell upon an inter-shelf route by using a shelf identifier (BTSI shelf number) and a slot identifier (slot identification number) (col. 10, lines 13-18). Timbs further discloses that, once a cell is received upon a particular destination shelf, the cell is routed according to a link identifier (span line number) and a channel identifier (channel number) (col. 10, lines 24-36). Timbs teaches that routing according to a shelf identifier, a slot identifier, a link identifier, and

a channel identifier is beneficial because this permits "near-static routing of a data stream" "with minimal requirements of shared resources" (col. 2, line 66-col. 3, line 3). Simply, in such a system, within the switch, each intermediate module will be able to switch a cell based on static information contained in the module (col. 3, lines 7-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to switch packets according to a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label in the system of Shiota since such routing permits "near-static routing of a data stream" where this eases the burden on the switch to update the switching tables.

26. Claims 12, 33, 38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiota (USPN 6,987,762), of record, in view of Shimojo et al. (USPN 5,787,072), of record.

27. Regarding claims 12 and 33, Shiota discloses an apparatus at a node of a network, comprising: a plurality of circuit cards and a switching fabric (Fig. 1 and col. 8, lines 39-41); means for receiving a packet, the packet being an IP packet and including a label stack, the label stack including an external routing label for use in forwarding between nodes along a label-switched path (col. 8, lines 39-59, where an MPLS packet is received and its label stack is processed, and col. 1, lines 26-28, where the MPLS packet is an IP packet "encapsulated by the data called a shim header"); means for pushing an internal routing label to the label stack of the packet (where a controller writes an "updated internal held header" to a packet, col. 15, lines 26-33, where the internal held header includes output channel information, col. 13, lines 38-48, and where the switch uses the output channel information to route the packet to the correct line card, col. 8, lines 43-55), means for routing a packet through the switching fabric to one of the

plurality of circuit cards based on an internal routing label attached to the packet (where a controller writes an "updated internal held header" to a packet, col. 15, lines 26-33, where the internal held header includes output channel information, col. 13, lines 38-48, and where the switch uses the output channel information to route the packet to the correct line card, col. 8, lines 43-55).

Shiota does not expressly disclose means for removing the internal routing label prior to transmission of the packet from the apparatus. Shimojo teaches, in a system utilizing an internal routing label, removing the internal routing label prior to the transmission of the packet from the apparatus (col. 1, lines 36-42, where the internal routing label is removed, i.e. "popped," before the cell is output). It is implicit that this is done to increase bandwidth efficiency in the network by removing information from the packet that will not be used by subsequent nodes. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to remove the internal routing label prior to transmission of the packet from the apparatus to increase bandwidth efficiency in the network.

28. Regarding claim 38, Shiota in view of Shimojo discloses that the internal routing label includes at least one field for identifying the location of one of the plurality of the circuit cards within the node (Shiota: col. 8, lines 51-55, where the switch switches the packets to a line card based on the output channel information, i.e. the input routing label, such that the output channel information must identify the location of one of the plurality of circuit cards within the node).

29. Regarding claim 40, Shiota in view of Shimojo discloses a memory for storing a routing table, the routing table including fields for the external label and the internal routing label

(Shiota: col. 9, lines 13-16, where the storing memory 15 stores the output channel information, i.e. the internal routing label, and a shim header group, i.e. an external label).

30. Claims 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiota (USPN 6,987,762), of record, in view of Shimojo et al. (USPN 5,787,072), of record, as applied to claim 33 above, and further in view of van Landegem (USPN 5,265,091), of record.

31. Regarding claim 34, Shiota in view of Shimojo does not expressly disclose a processor, the processor including means for sending a reply packet in response to receiving a control packet to one of the plurality of circuit cards identified in the internal routing label. However, Shiota in view of Shimojo does disclose setting up label switched paths through the apparatus (Shiota: col. 2, lines 1-16). Van Landegem teaches, in a system utilizing internal routing labels, using a processor (Fig. 4, ref. PR113), the processor including means for sending a reply packet in response to receiving a control packet to one of the plurality of circuit cards identified in the internal routing label (col. 9, lines 45-52, where the processor sets a VP and a new routing field for a control cell, and col. 10, lines 6-14, where a confirm control cell containing the VP and routing field are returned to the sender to acknowledge the setup of the connection). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a processor, the processor including means for sending a reply packet in response to receiving a control packet to one of the plurality of circuit cards identified in the internal routing label in order to set up label switched paths through the apparatus.

32. Regarding claim 35, Shiota in view of Shimojo in further view of van Landegem discloses that the internal routing label further includes a packet type identifier (van Landegem: col. 8, lines 28-34).

33. Regarding claim 36, Shiota in view of Shimojo in further view of van Landegem discloses that the means for routing also routes based, at least in part, on the packet type identifier (van Landegem: col. 9, lines 12-17, where the node switches control packets to a processor and Shimojo: col. 1, lines 36-42, where the node switches normal packets to a destination circuit card).

34. Regarding claim 37, Shiota in view of Shimojo in further view of van Landegem discloses that the means for routing includes means for routing the packet to the processor if the packet type identifier indicates a control packet type (van Landegem: col. 9, lines 12-17, where the node switches control packets to a processor and Shimojo: col. 1, lines 36-42, where the node switches normal packets to a destination circuit card).

35. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiota (USPN 6,987,762), of record, in view of Shimojo et al. (USPN 5,787,072), of record, as applied to claim 38 above, and further in view of Timbs (USPN 5,809,025), of record.

36. Regarding claim 39, Shiota in view of Shimojo does not expressly disclose that the field for identifying the location of one of the plurality of circuit cards within the node includes identifiers for a shelf and a slot of the one of the plurality of circuit cards. Timbs teaches, in a system for switching cells between cards, routing a cell upon an inter-shelf route by using a shelf identifier (BTSI shelf number) and a slot identifier (slot identification number) (col. 10, lines 13-18). Timbs teaches that routing according to a shelf identifier and a slot identifier is

beneficial because this permits "near-static routing of a data stream" "with minimal requirements of shared resources" (col. 2, line 66-col. 3, line 3). Simply, in such a system, within the switch, each intermediate module will be able to switch a cell based on static information contained in the module (col. 3, lines 7-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to switch packets according to a shelf identifier and a slot identifier included in the internal routing label in the system of Shiota since such routing permits "near-static routing of a data stream" where this eases the burden on the switch to update the switching tables.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The examiner can normally be reached on Mon.-Fri. 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel J. Ryman
Examiner
Art Unit 2616

Daniel Ryman